Claims

[c1] 16. A method of fabricating a flash memory device, comprising the steps of:
providing a first conductive type substrate having a second conductive type first well already formed therein;
forming a liner layer and a mask layer over the substrate sequentially;
patterning the mask layer, the liner layer and the substrate to form an opening in the substrate;
forming a tunnel dielectric layer over the interior surface of the opening;
forming a first conductive type pocket doping region within the substrate on the sidewall of the opening:
forming a first floating gate and a second floating gate on the sidewalls of the opening;
forming a source region in the substrate at the bottom section of the opening;
forming an inter-gate dielectric layer inside the opening;
forming a first control gate and a second control gate on the sidewalls of the opening such that the first control gate extends to cover the sidewall of the first floating gate and the second control gate extends to cover the sidewall of the second floating gate;

removing the mask layer and the liner layer;
forming a source region in the substrate;
forming a first conductive type second well region within the second conductive type first well region such that the junction between the first conductive type second well region and the second conductive type first well region is at a level higher than the bottom section of the opening;
forming an insulating layer in the space between the first control gate and the second control gate and forming a spacer on the sidewall of the first control gate and the second control gate;
forming an inter-layer dielectric layer over the substrate;
forming a contact inside the inter-layer dielectric layer so that the contact connects the drain region with the first conductive type second well region to form a short-circuit; and
forming a conductive layer over the inter-layer dielectric layer such that the conductive layer and the contact are electrically connected.

[c2] 17. The method of claim 16, wherein the step of forming a first conductive type pocket doping region in the substrate on the sidewall of the opening further comprises implanting ions at a slant angle.

[c3] 18. The method of claim 16, wherein the step of forming a first floating gate and a second floating gate on the

sidewalls of the opening further comprises the steps of:
forming a first conductive layer over the substrate such that the opening is completely filled;
removing a portion of the first conductive layer so that the upper surface of the first conductive layer is slightly below the upper surface of the substrate;
forming a second spacer on the sidewalls of the mask layer;
removing a portion of the first conductive layer using the mask layer and the second spacers as a mask; and
removing the second spacer.

[c4] 19. The method of claim 16, wherein the step of forming a first control gate and a second control gate on the sidewalls of the opening further more comprises the steps of:
forming a second conductive layer over the substrate such that the opening is completely filled;
removing a portion of the second conductive layer such that the upper surface of the second conductive layer is at a level lower than the upper surface of the mask layer but higher than the floating gate;
forming a third spacer on the sidewalls of the mask layer;
removing a portion of the second conductive layer using the mask layer and the third spacer as a mask; and

removing the third spacer.

[c5] 20. The method of claim 16, wherein the step of forming an insulating layer in the space between the first control gate and the second control gate and the first spacers on the sidewalls of the first control gate and the second control gate further comprises:
forming an insulating material layer over the substrate such that the space between the first control gate and the second control gate is completely filled; and
performing an anisotropic etching process to remove a portion of the insulating material layer.